



ALTERNATIVE TO PTO/SB/06A/B (09/06)

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				First Named Inventor	Bruce W. MCGAUGHEY
				Art Unit	2123
				Examiner Name	A. Pierre-Louise
Sheet	1	of	1	Attorney Docket Number	188122001900

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
APL	1.	US-2003/0237067-A1	12-25-2003	Mielke et al.	
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		Country Code ³ -Number ⁴ -Kind Code ⁵ (if known)			
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NON PATENT LITERATURE DOCUMENTS					
Examiner Initials	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²		
	12.	Chakrabarti, D.R. et al. (November 23-24, 1995). "An Improved Hierarchical Test Generation Technique for Combinational Circuits with Repetitive Sub-circuits," <i>Proceedings of the Fourth Asian Test Symposium 1995</i> , 1:237-243.			
	13.	Jones et al. (February 1994). "A Cache-Based Method for Acceleration Switch-Level Simulation," <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , 13(2).			
	14.	Stanford.edu. "Radix 2 FFT Complexity is N Log N," <i>In Mathematics of the Discrete Fourier Transform (DFT), with Music and Audio Application</i> . Smith, III, J.O. (2003). W3K Publishing: Stanford, located at < http://ccma.stanford.edu/~jos/mdft/Radix_2_FFT_Complexity.html >, 1 page.			
	15.	Wong, Y. (1985). "Hierarchical Circuit Verification," <i>IEEE 22nd Design Automation Conference</i> .			

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Examiner Signature		Date Considered	7/21/2007
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